Operational-Amplifier Design

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EE 420: Analog Integrated Circuit Design
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Project Details

Using On Semiconductor's 500 nm process (C5 with two polysilicon layers and 3 levels of metal with a lambda of 300 nm) design an op-amp that can operate with a VDD down to 2 V while driving 100 pF (maximum) and 1kΩ (minimum) load.

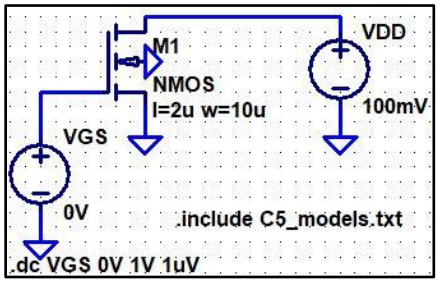
Design Constraints:

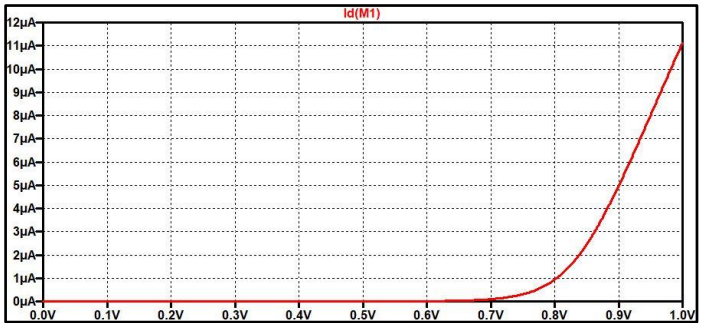
1. DC open-loop gain > 66 dB
2. Gain-bandwidth product > 1 MHz
3. Common-mode rejection ratio > 90 dB at 100 kHz
4. Power supply rejection ratio > 60 dB at 1 kHz
5. Slew-rate with maximum load > 1 V/µs

MOSFET Characterization

In order to start the design, I must first be able to characterize the C5 model. This must be done in order to size the devices and bias them correctly so that they are all in saturation. The first circuit I will build will be to find the threshold voltage of both the NMOS and PMOS. Since the devices we are using are of the short-channel process, I am going to refer to Chapter 9 of the course textbook, "Circuit Design, Layout, and Simulation, Third Edition" by Dr. R. Jacob Baker.

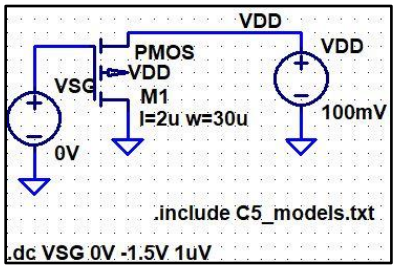
- NMOS Threshold Voltage

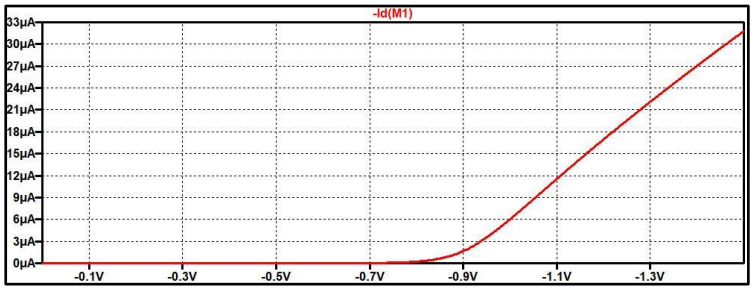




Looking at the plot above, if I drew a straight line as it becomes linear, the line would touch the x-axis at approximately 800mV. Therefore, I can characterize the threshold voltage of the NMOS, **V_{THN} = 800mV**.

- PMOS Threshold Voltage





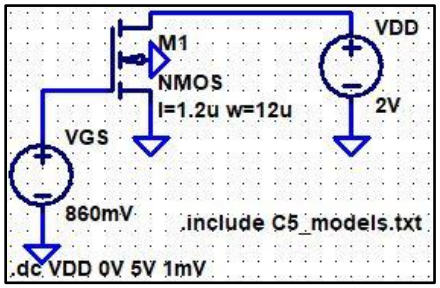
Same for the NMOS, the PMOS threshold voltage, we find it by looking at where the line crosses the x-axis. In this case, it looks like it crosses the x-axis at -900mV. Therefore, I can characterize the PMOS threshold voltage, **V_{THP} = -900mV**.

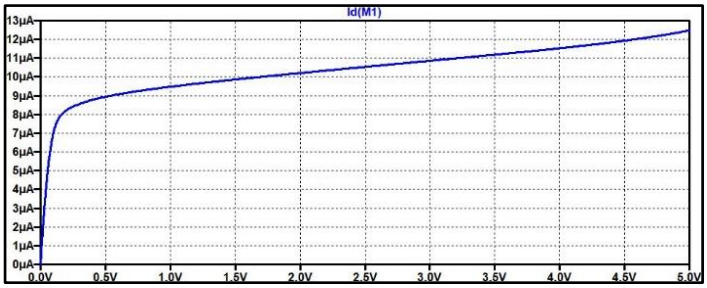
- Finding V_{GS} and V_{SG}

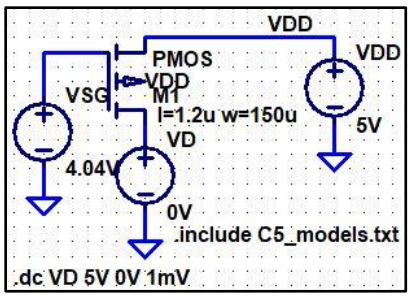
Being able to find the V_{SG} and V_{GS} needed to bias the MOSFETs correctly is something simple. Referring to the course textbook, general analog design for short-channel MOSFETs calls for roughly 5% of V_{DD} for the overdrive voltage. We know that for overdrive voltage: $V_{OV} = V_{GS} - V_{THN}$. The overdrive voltage should be less than 5% of V_{DD} so I will choose it to be 3% of V_{DD}. This means that V_{OV} = 60mV. Rearranging the above equation to solve for V_{GS} and V_{SG} gives me: **V_{GS} = 860mV** and **V_{SG} = 960mV**.

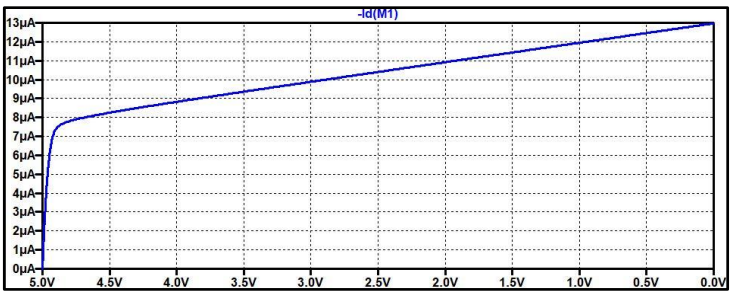
- Finding W

In order to find what these values should be for a specific current, I must first choose what bias current I want. For this design, I will be choosing a bias current, I_D = 10 µA. This was chosen because the bias current heavily affects the slew rate and there is a capacitive load. Since we are trying to achieve a slew-rate that is greater than 1 V/µs, a bias current of 10µA is appropriate. Now that I have chosen an appropriate bias current, I can then find the size for W that I want. I will show my selection of W by use of LTSpice simulation.









Looking at the simulations above we can see that I am selecting my NMOS **W = 12 µm** and my PMOS **W = 150 µm**.

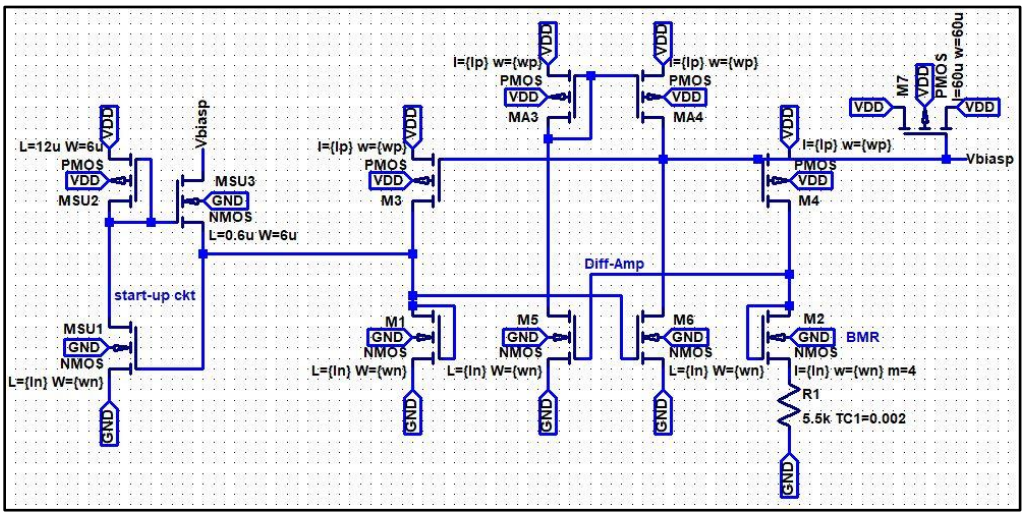
- Finding L

  To find the appropriate L size, I referred to the course textbook which explains that, as a good starting point, the length of the devices should be twice that of the minimum length. The minimum length for the C5 process is 0.6 µm; as such, I started off with my device lengths as **L = 1.2 µm**. It will be shown later that I needed to change the length of my devices to be the minimum length since my op-amp required more speed to fulfill the slew-rate constraint.

Biasing Circuit Design

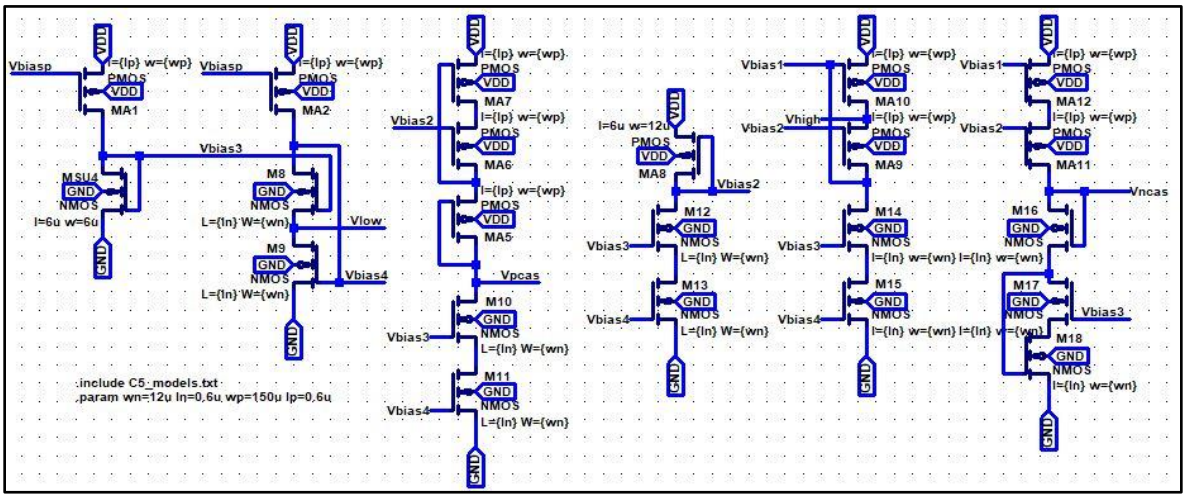
In order to bias the op-amp circuit correctly, I need to use a self-referenced bias circuit so that when V_{DD} is changed, it does not affect the op-amp circuit. After reading through the textbook, I concluded that it would be best to use a general biasing circuit for short-channel design. This biasing circuit includes a start-up circuit, BMR, and a diff-amp to provide a bias voltage to the rest of the biasing circuit which in turn provides bias voltages to the op-amp circuit.

- Start-Up, BMR, and Diff-Amp Circuit



The sizes of the devices used above can be found in the figure below.

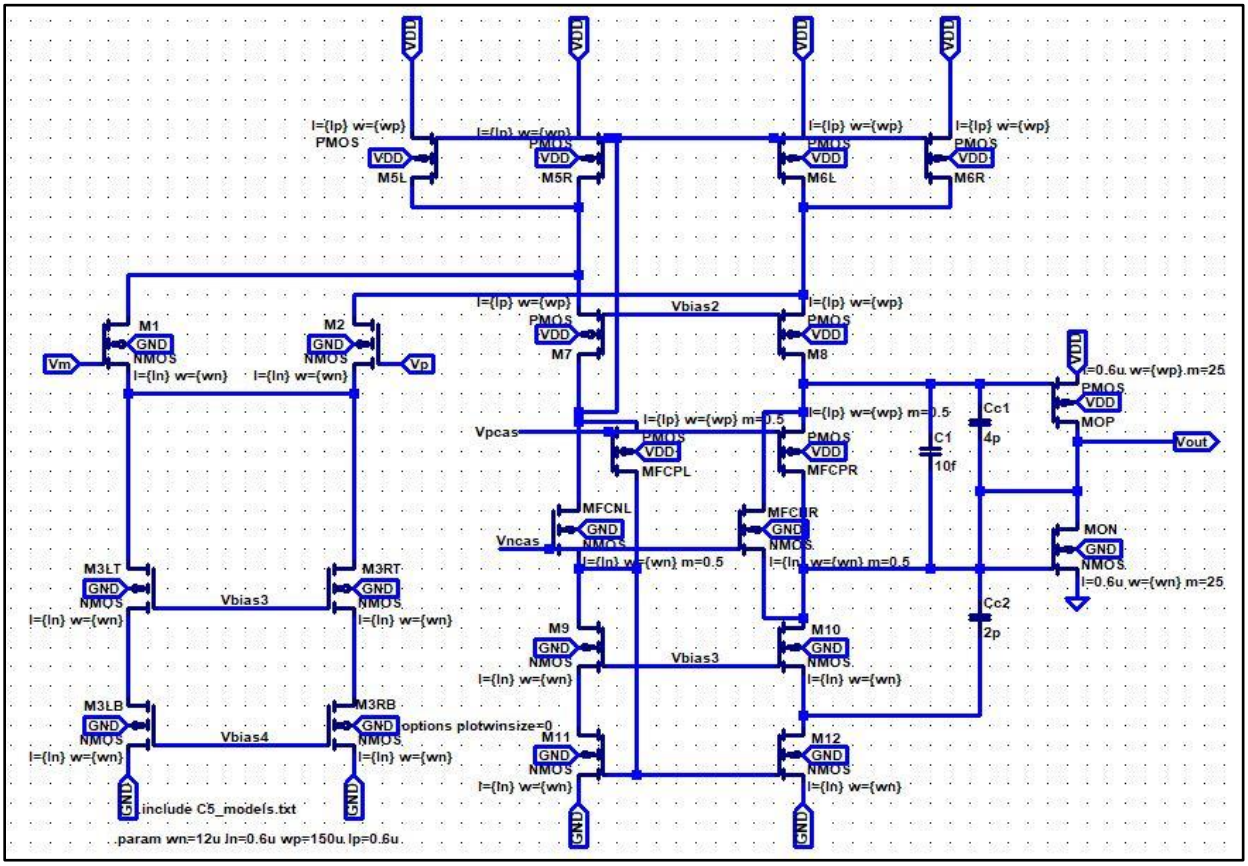
- Wide-Swing Cascode Current Mirrors



The BMR above uses PMOS devices to supply the reference current for biasing. The circuit uses a diff-amp to force the current to be more stable since the output resistance increases. The bias voltage then sets the current to be flowing in the current mirrors. These current mirrors are in a wide-swing cascode topology. These current mirrors provide the appropriate bias voltages for my op-amp design.

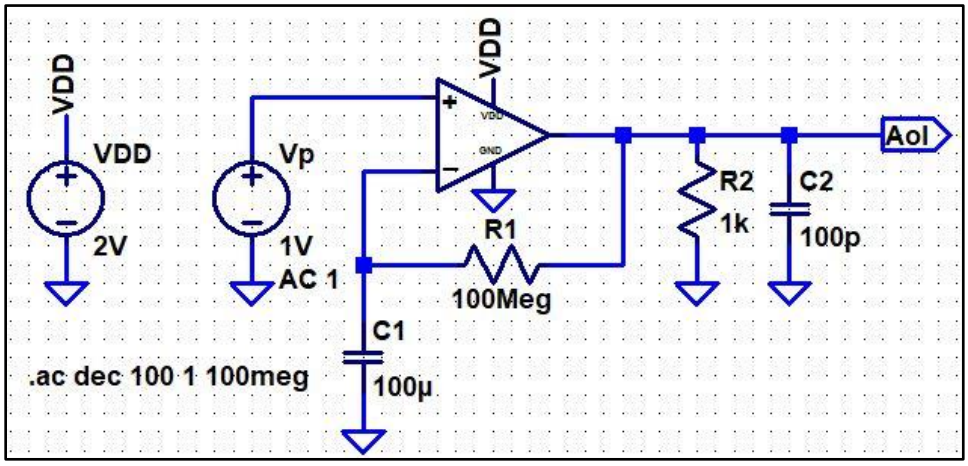
Op-Amp Design

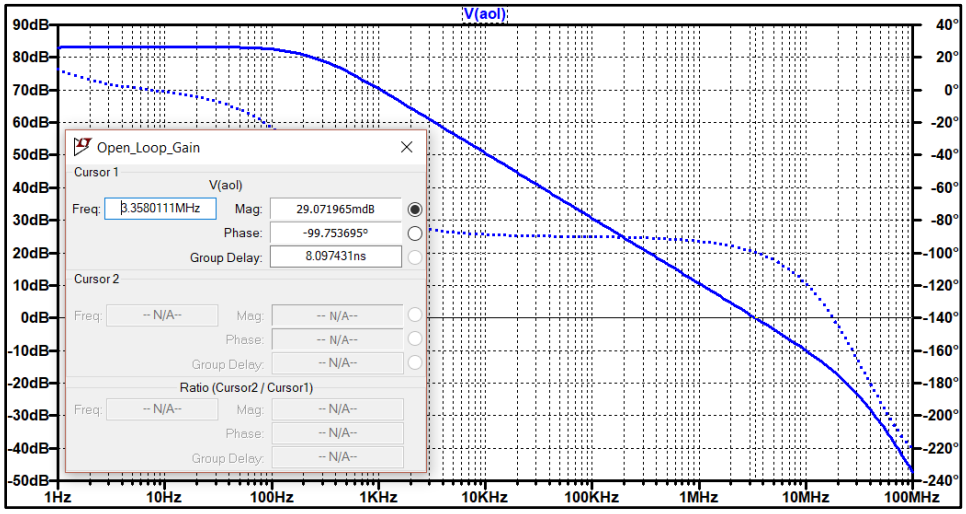
My op-amp design is of a folded-cascode with class AB output buffer topology. First, the folded-cascode structure is constructed to provide the bias current that I am looking for. The folded-cascode structure includes floating current sources which are MFCPL, MFCNL, MFCPR, and MFCNR below. These devices are half of the device size selected from above. That means that these devices steal only half of the current from the PMOS devices above, which are M5L, M5R, M6L, and M6R. They are biased using V_{pcas} and V_{ncas}. This helps equalize the voltages across M9 and M10. The input to the op-amp are devices that are simply stealing current from the PMOS devices above. The devices M3LT, M3LB, M3RT, and M3RB will be biased using the biasing circuit from above to steal the current needed for M1 and M2 to stay in saturation. The gates of M1 and M2 are the inputs to the op-amp, V_m and V_p, respectively. The output stage of this design is the class AB output buffer. These devices, MOP and MON, are what provide the gain necessary. These devices are sized accordingly to increase or decrease gain. The PMOS will source the current and the NMOS will sink current. The capacitor, C1, is used to tie the gates of the output buffer together during AC operation. This helps the voltages move together and will keep the power dissipation of the op-amp low. The capacitors, Cc1 and Cc2, help with compensating the op-amp to control the stability of the circuit; which will be shown using a step response later. Shown below, in order to get a high enough DC open-loop gain, I had to increase the sizes of the MOSFETs of the output stage.



DC Open-Loop Gain

Since I cannot ground the inverting terminal of the op-amp, I will place a big resistor between the inverting terminal (V_m) and V_{out}, and then place a big capacitor from the terminal to ground. This will not allow any feedback to the inverting terminal, thus simulating open-loop frequency response. I will apply a small-signal to the non-inverting terminal (V_p) and perform an AC analysis. From the plot, I will be looking at the lowest frequency for the DC open-loop gain, and then we can observe the unity gain frequency, f_{un}, as well.

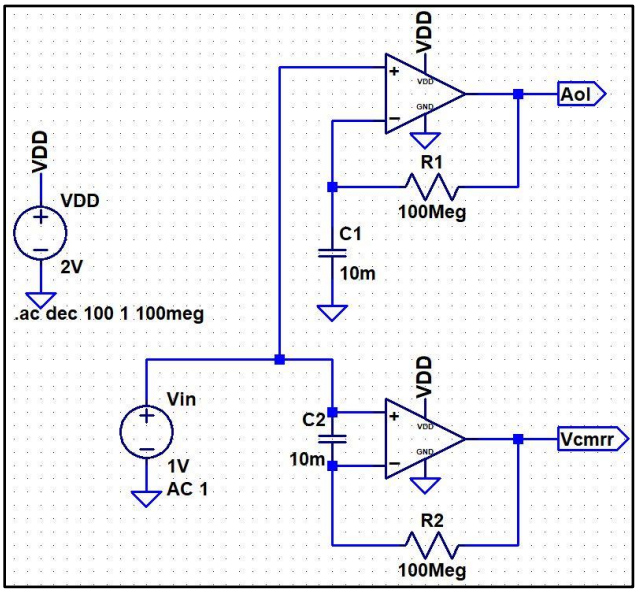


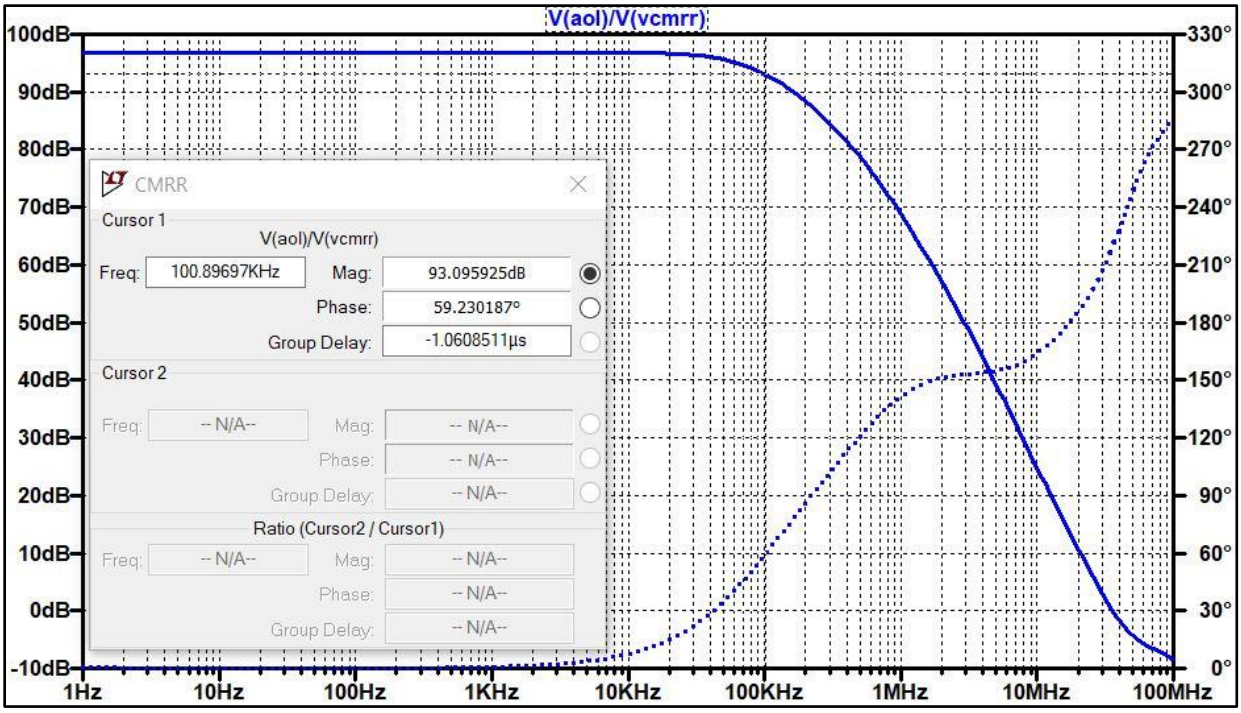


It is observed that the DC open-loop gain for my op-amp is **> 80dB**. The plot above also shows that at the unity gain frequency, I have a phase of -99.75º. This gives me a phase margin of **PM = -99.75º - (-180º) = 80.25º**. The closer the phase margin is to 90º means the more of a first order response the circuit will have. When I show the step response later, we will see that the op-amp has a stable step response that looks like an RC circuit (where the output takes time to follow the input voltage. Also, at unity gain frequency, which is: f_{un} = Gain * Bandwidth, is my gain-bandwidth product (GBP). My **GBP = 3.36 MHz**, which meets the specification for the project.

Common-Mode Rejection Ratio

The CMRR is important because analog systems, oftentimes, transmit signals differentially. The ability of the op-amp to reject the common-mode noise is something worth looking at. The larger that a designer can get the CMRR to be, the op-amp will perform better. The design constraint for this was that the CMRR > 90 dB at 100 kHz.

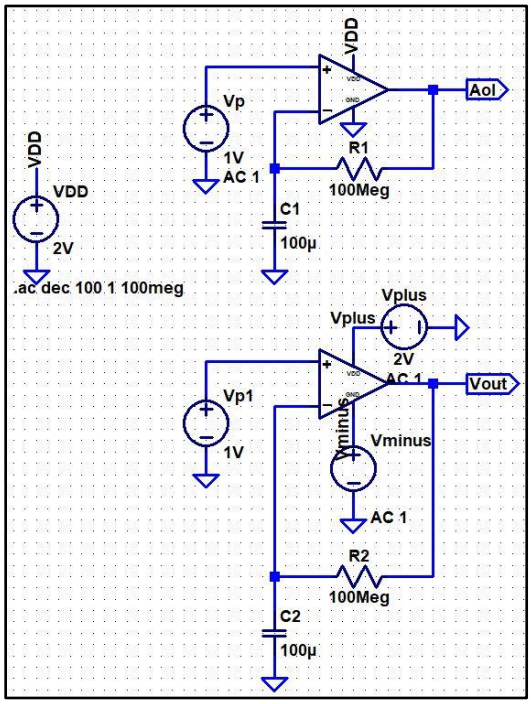


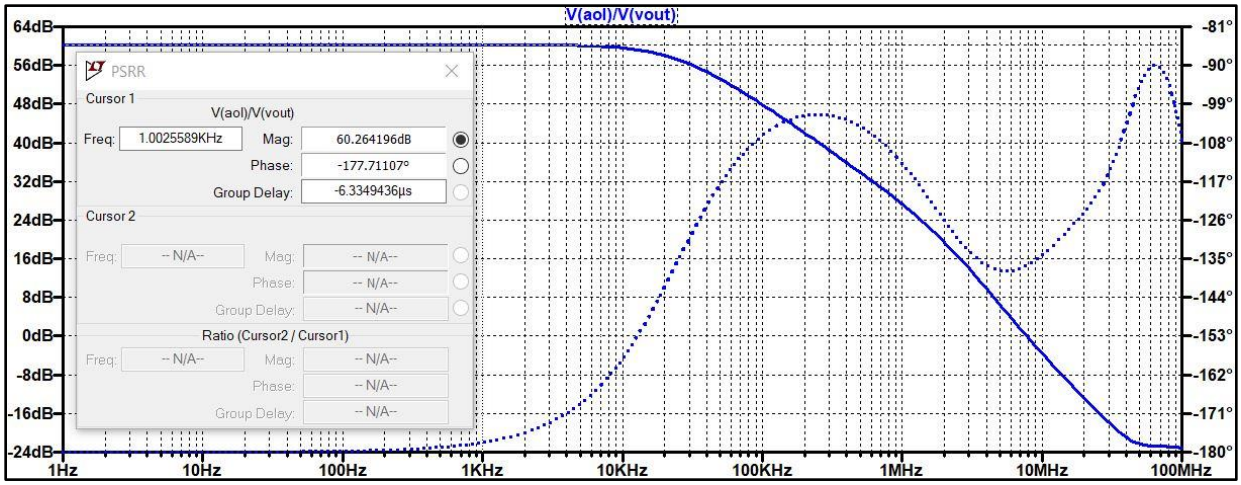


I simulated a CMRR of approximately **93 dB at 100 kHz**.

Power Supply Rejection Ratio

This parameter for an op-amp describes how well it can reject changes in V_{DD} or noise from the power supply, including the ground. The output voltage could vary when this happens and is unwanted for whatever application the op-amp is being used for. The higher the designer can make the op-amp's PSRR, the performance will be better.

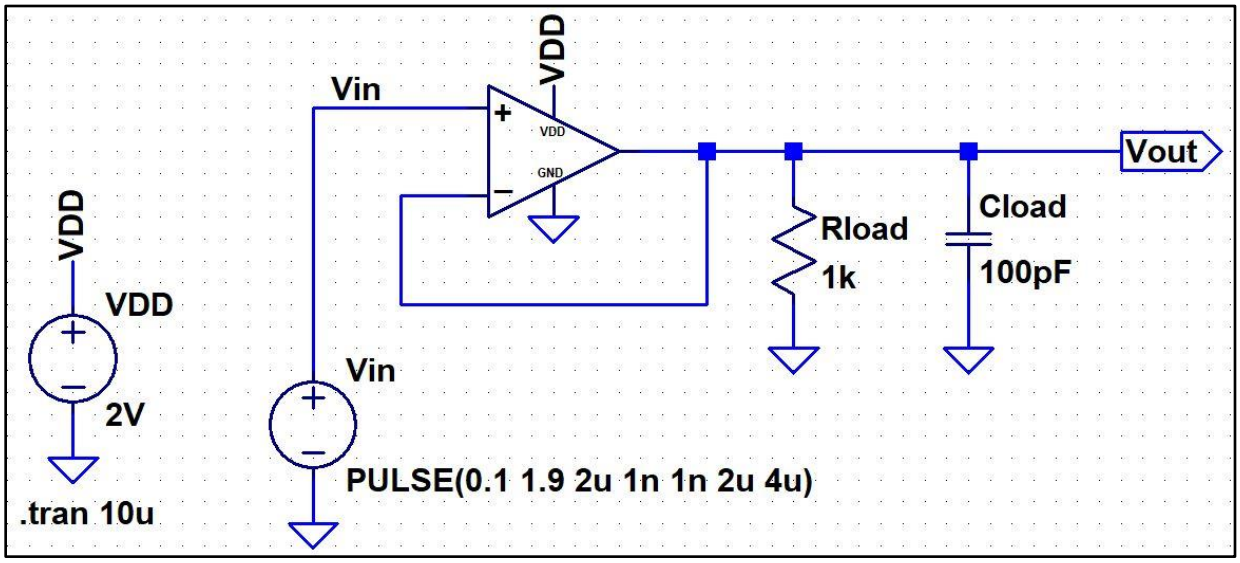


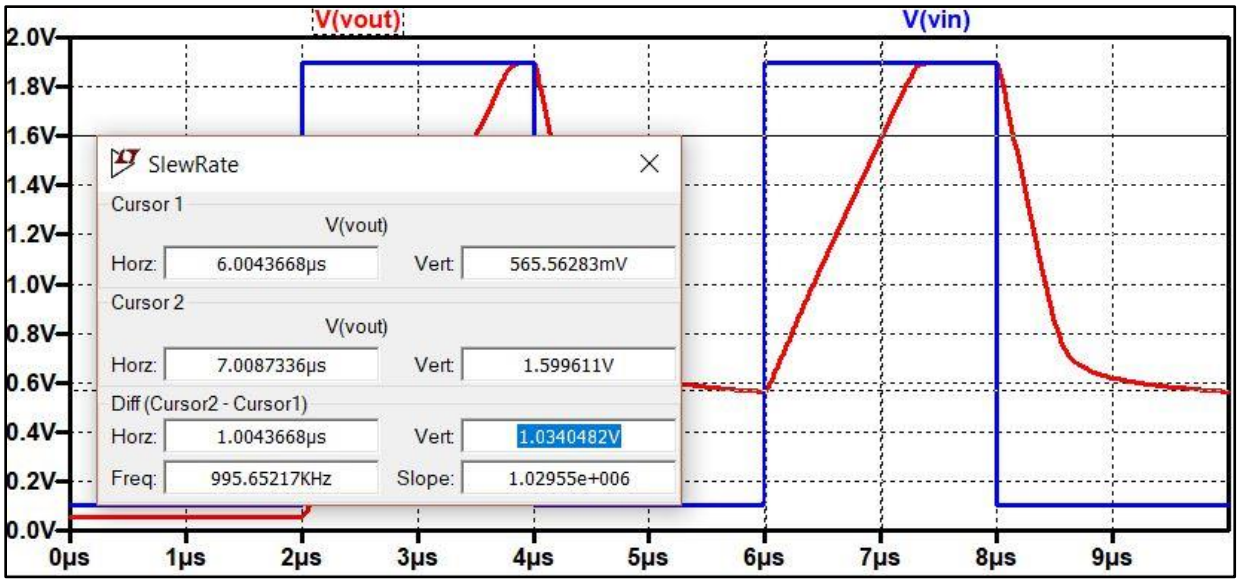


The PSRR of my op-amp is simulated to be **60.26 dB at 1 kHz**, which meets the specification for this project. I believe, that given more time, I would be able to understand the project quite a bit more and be able to increase this while keeping all of the other parameters within the constraints.

Slew-Rate

The slew-rate is an important factor to consider for an op-amp since this is how the speed of an op-amp can be characterized. This rate is how quickly the op-amp can change the output to what it needs to be given an abrupt change at the input. Generally, the faster the slew-rate, gain will be sacrificed.

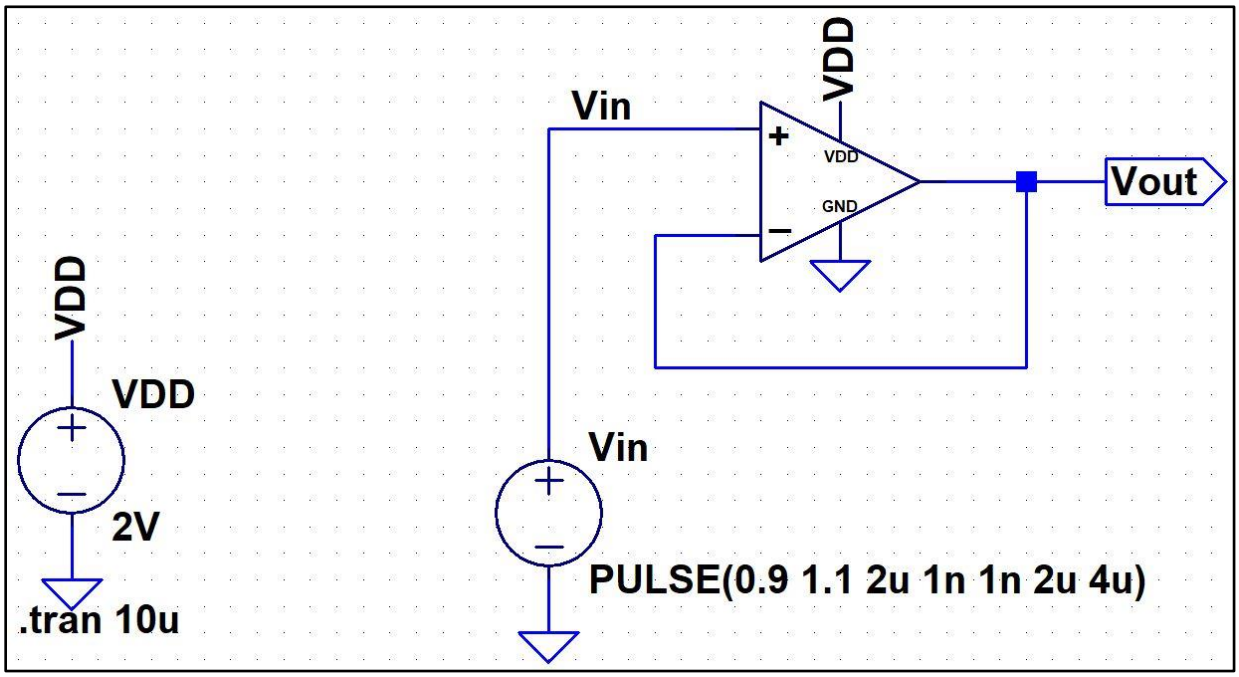


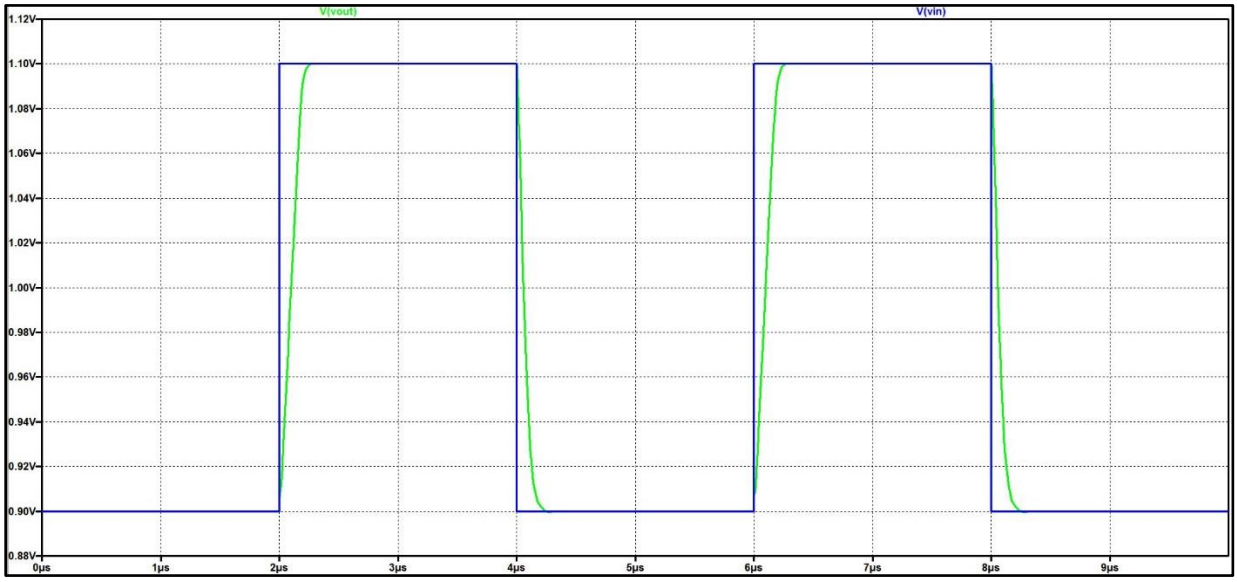


The plot above shows that my slew rate is just slightly larger than 1V/µs, **Slew-Rate = 1.034V/µs**. This is something that could be improved with my design. I changed the lengths of my devices to the minimum size just to meet this requirement. With a length 2 times that of the minimum, I was simulating 800-900mV/µs for my first few design iterations. With that being said, if more time was available, I would look more into making the slew-rate much faster without sacrificing too much gain.

Step Response

The step response of the op-amp is a clear way to show stability. If there is an overshoot when a step input is applied, it is an indicator that the op-amp is unstable. This means that the response is not a first-order response. A first-order response means that the op-amp is going to respond in a manner where it does not overshoot, rather, it will follow the input in a "calm" manner. It will respond like the charging and discharging of a capacitor in an RC circuit.

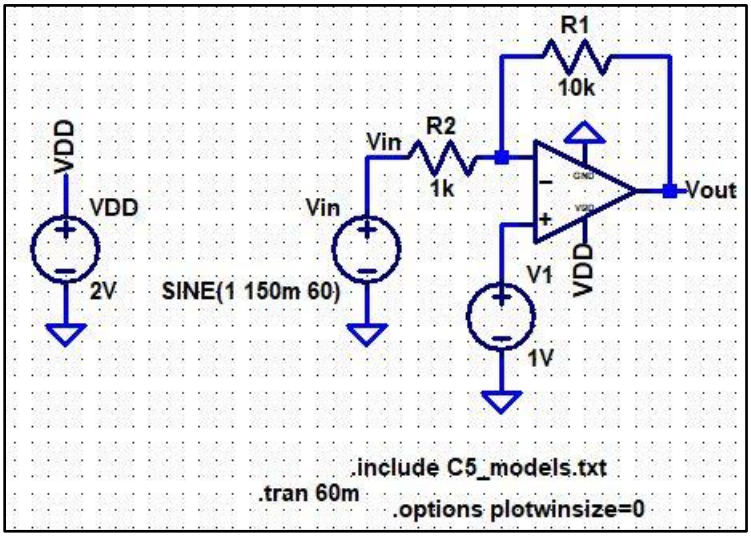


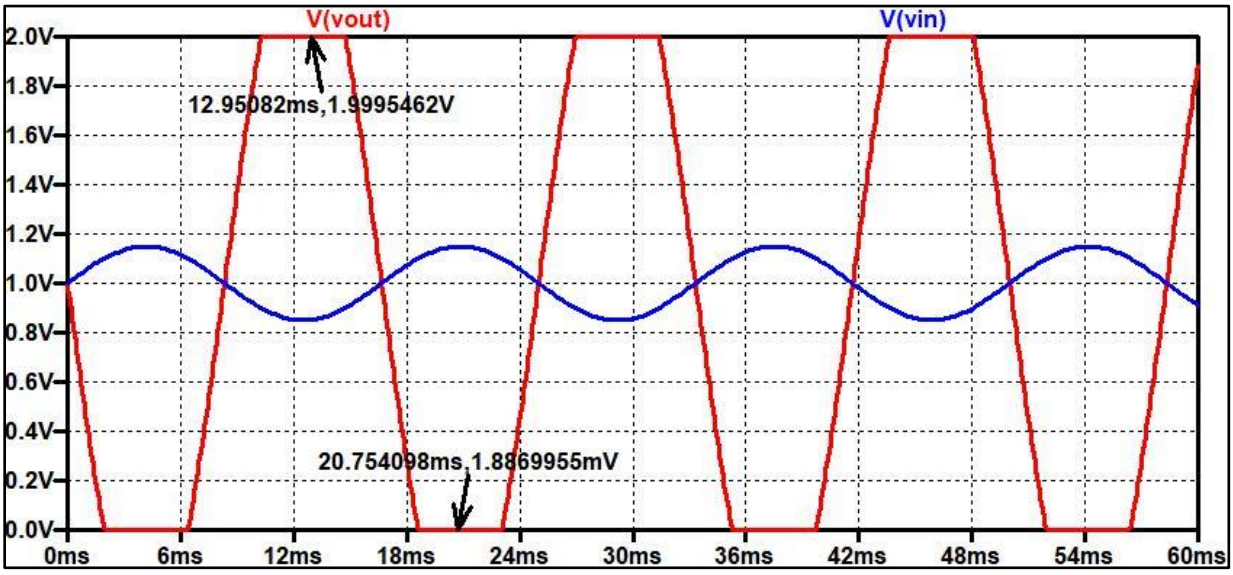


The circuit has a stable, first-order response.

Output Swing

I simulated the output swing of this op-amp and the simulations below show how large of a swing my op-amp design has.

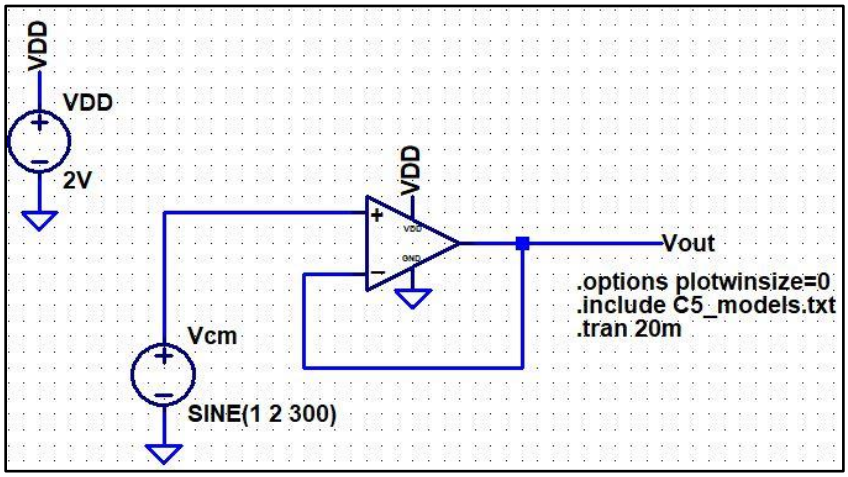


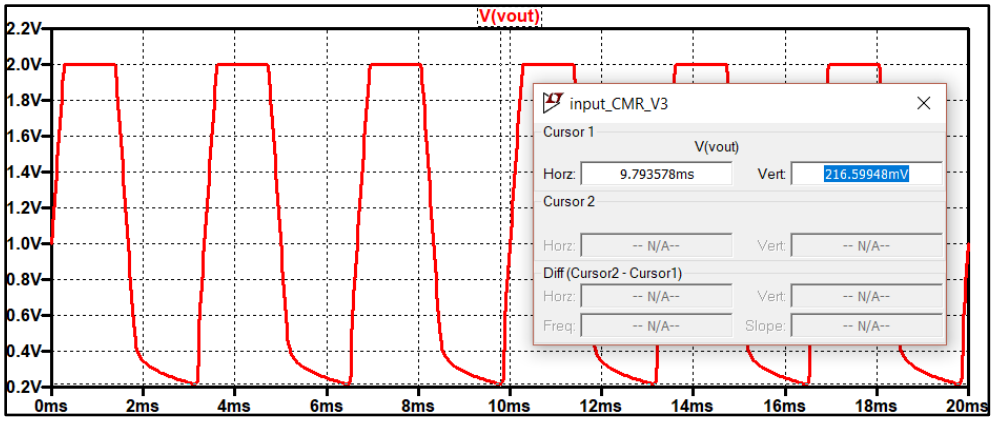


It looks like the output swing ranges from **~1.9mV to ~1.99V**. This means that the minimum voltage output will be whatever voltage is attached to GND of the op-amp plus 0.114mV. The maximum will be whatever voltage is attached to V_{DD} of the op-amp minus 1mV

Input CMR as a function of V_{DD}

The input common-mode range is how high the common-mode voltage (average of voltages between the inverting and non-inverting inputs of the op-amp) or low the common-mode voltage can be. This is important to know because the user of the op-amp would need to know if my op-amp is suitable for their circuit.





Performing circuit analysis to solve for the gate voltage of V_p or V_m from V_{DD} will give me the maximum input common-mode voltage.

$$V_{cm,max} = VDD - V_{OV} - V_{GS} = 2V - 0.06V - 0.86V = 1.08V$$

And so, this means that the maximum input common-mode voltage can be 1.08 V higher than the power supply.

Doing the same circuit analysis starting from ground will give me the minimum input common-mode voltage.

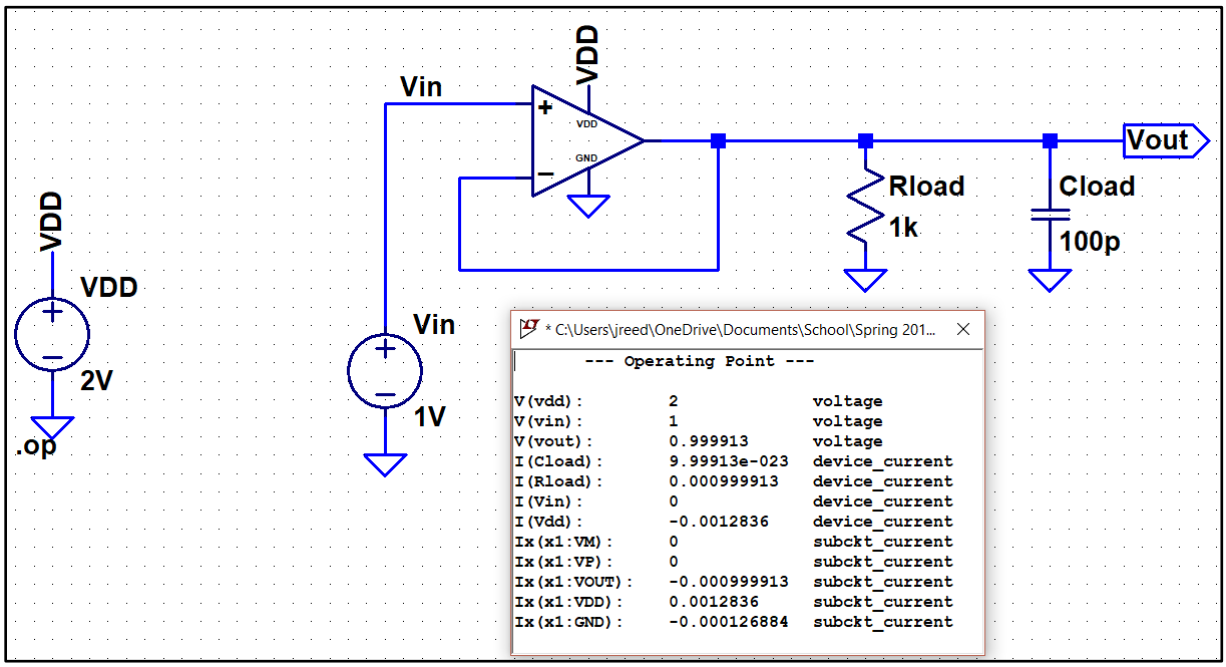
$$V_{cm,min} = V_{OV} - V_{THN} = 0.06V - 0.8V = -0.74V$$

This means that the minimum input common-mode voltage can be 0.74 V below ground.

Looking at the plot above shows that the positive cycle of the waveform clips at approximately 2 V and the negative cycle clips at approximately 0.217V. When I subtract the DC offset from these numbers, I get the maximum and minimum input common-mode voltages solved above.

Power Dissipation

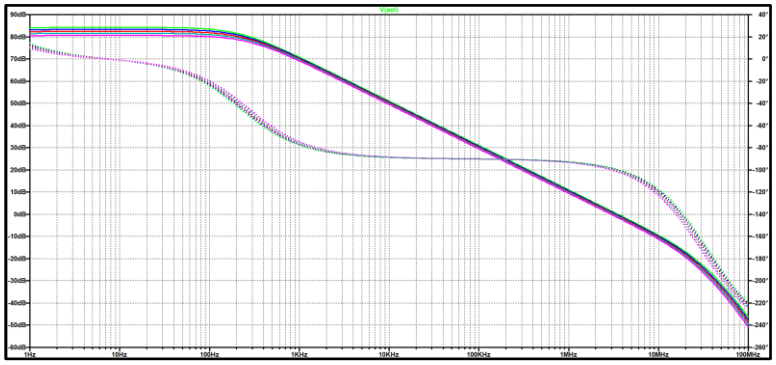
To find the power dissipation, I just set up a voltage follower topology with the load attached and simulated the DC operating point. I was able to see the current draw from V_{DD}, and I can just multiply V_{DD} by the current simulated to find the power dissipation of the op-amp.

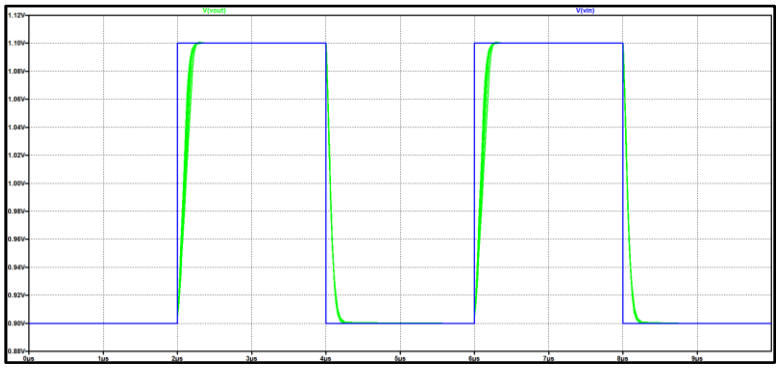


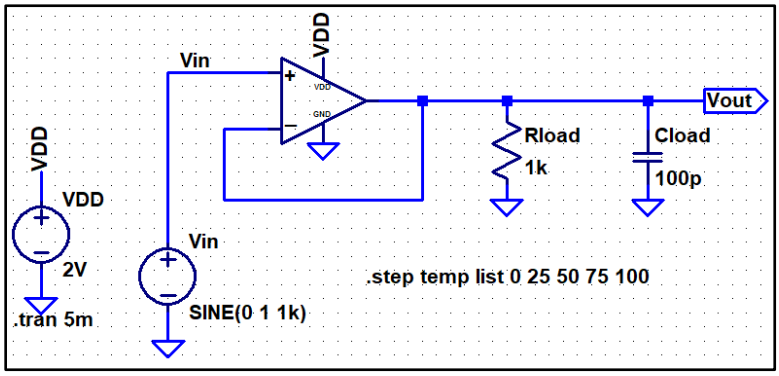
We can see the current through V_{DD} to be approximately 1.28mA. This means the power dissipated is **P = (2V)*(1.28mA) = 2.56mW**.

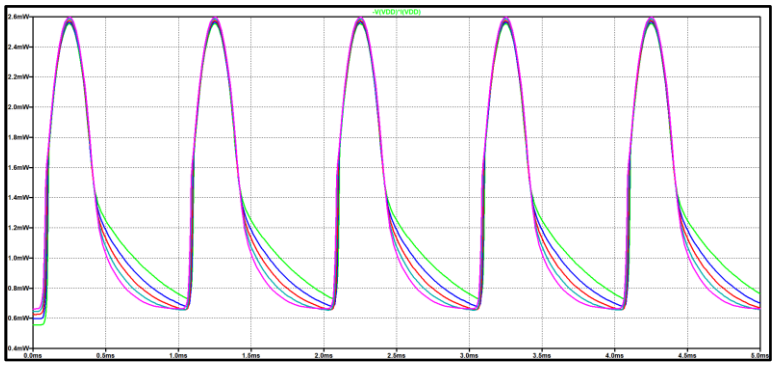
Temperature Behavior

I want to document how the DC open-loop gain, step response, and power dissipation are affected by changes in temperature.









Looking at the plots above, I am confident that with major temperature changes, the behavior of my op-amp does not vary its performance too much.

Conclusion

The design of an operational-amplifier can be difficult if one does not know how to manipulate the circuit layout of devices and device sizing. The most challenging part for me was being able to find the correct sizes for my devices and choosing the right compensating capacitors. When I made one parameter meet specification, another parameter would become worse. I had to refer to the course textbook several times and read about how device sizing affects gain and speed. The project was personally rewarding because op-amps have always been mysterious with the fact that we use a block diagram and assume they are ideal when performing circuit analysis. When reading the datasheets for several op-amps, I did not know what the parameters meant. I now not only know what the parameters mean, I have learned how to control what the parameters will be to design an op-amp for any purpose.

Summary of Results Table

Values found at $V_{DD} = 2V$

DC open-loop gain, Load: 1kΩ, 100 pF	83.03 dB
Gain-Bandwidth Product/Unity Gain Frequency, Load: 1kΩ, 100 pF	3.358 MHz
CMRR @ 100 kHz	93.1 dB
PSRR @ 1 kHz	60.26 dB
Slew-Rate, Load: 1kΩ, 100 pF	1.034 V/µs
Output Swing	Min: GND + 0.114mV Max: V_{DD} – 1mV
Input CMR	$V_{cm,max:}$ V_{DD} + 1.08 V, $V_{cm,min}$ = GND – 0.74 V
Power Dissipation	2.56 mW